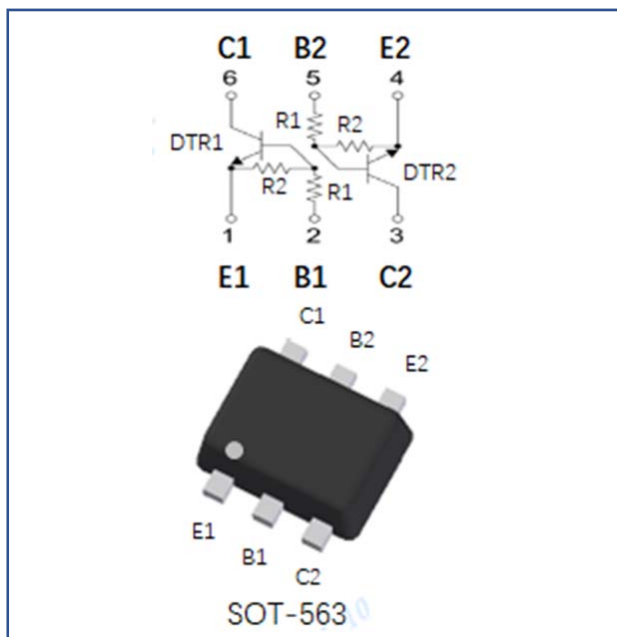


Dual NPN Digital Transistors (Built-in Resistors)



Features

- Moisture sensitivity level 1
- Halogen free and RoHS compliant
- Surface mount package ideally suited for automatic Insertion

Application

- Signal amplification
- Switching circuit

Mechanical data

- **Package:** SOT-563
- **Terminals:** Tin plated leads, solderable per J-STD-002 and JESD22-B102

■ Maximum Ratings (T_a=25°C Unless otherwise specified)

Item	Symbol	Unit	Conditions	Value
Device marking code				H9
Supply voltage	V _{CC}	V		50
Input voltage	V _{IN}	V		-6 to +40
Output current	I _O	mA		100
Power dissipation	P _D	mW		150
Junction temperature	T _J	°C		-55 to +150
Storage temperature	T _{STG}	°C		-55 to +150

**■ Electrical Characteristics** ($T_a=25^{\circ}\text{C}$ Unless otherwise specified)

Item	Symbol	Unit	Conditions	Min	Typ	Max
Input voltage	$V_{I(off)}$	V	$V_{CC}=5V, I_c=100\mu A$	0.3		
	$V_{I(on)}$	V	$V_o=0.3V, I_c=1mA$			1.4
Output voltage	$V_{O(on)}$	V	$I_o / I_i = 5mA / 0.25 mA$			0.3
Input current	I_i	mA	$V_i=5V$			0.88
Output current	$I_{O(off)}$	μA	$V_{CC}=50V, V_i=0$			0.5
DC current gain	G_i		$V_o=5V, I_o = 5mA$	68		
Input resistance	R_1	$k\Omega$		7	10	13
Resistance ratio	R_2/R_1			3.7	4.7	5.7
Transition frequency	f_T	MHz	$V_{CE}=10V, I_E=5mA, f=100MHz$		250	

■ Thermal Characteristics

Parameter	Symbol	Unit	Value
Thermal resistance, junction-to-ambient	$R_{\theta J-A}^{(1)}$	$^{\circ}\text{C/W}$	833
Thermal resistance, junction-to-case	$R_{\theta J-C}^{(1)}$	$^{\circ}\text{C/W}$	667

Note: Thermal resistance from junction to ambient and from junction to lead mounted on P.C.B. with 25.4mm*25.4mm copper pad areas

■ Ordering Information

Preferred P/N	Packing code	Unit weight(g)	Minimum package(pcs)	Inner box quantity(pcs)	Outer carton quantity(pcs)	Delivery mode
EMH9	F2	Approximate 0.0035	3000	30000	120000	7" reel

■Characteristics

Fig 1: DC Current Gain Characteristics

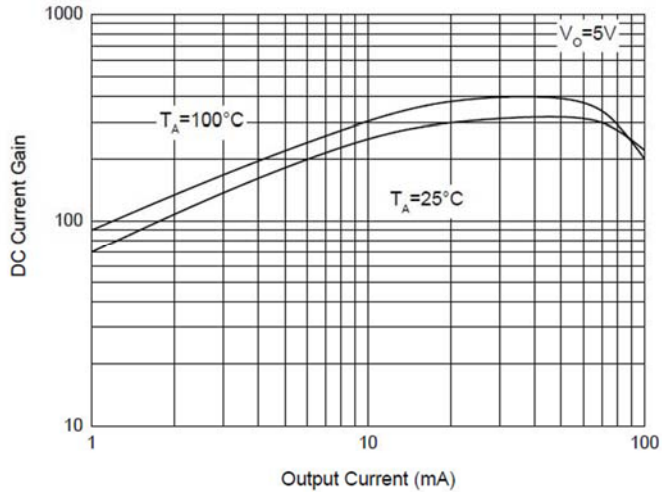


Fig 2: Input Voltage (On) Characteristics

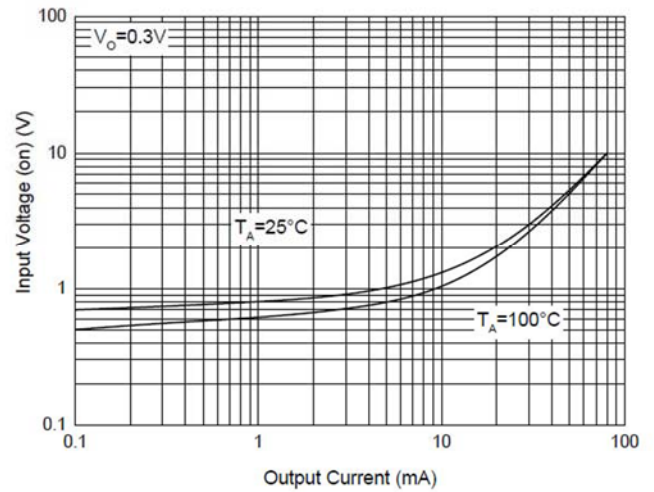


Fig 3: Input Voltage (Off) Characteristics

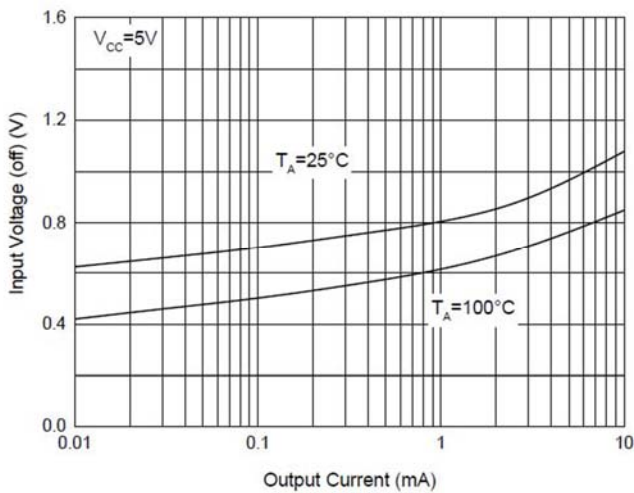


Fig 4: Output Voltage Characteristics

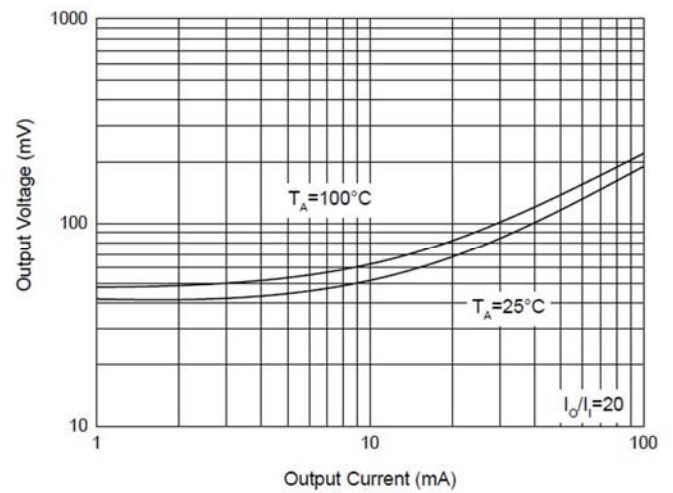
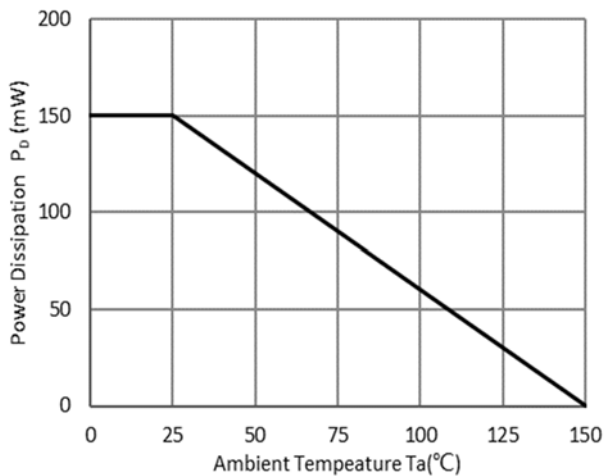
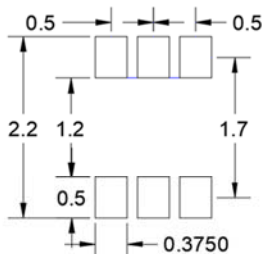
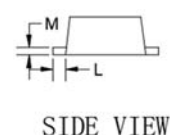
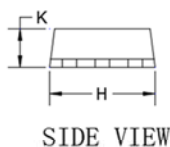
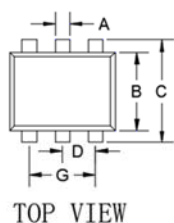


Fig 5: PD-Ta Curve



■ Outline Dimensions

SOT-563



单位: mm

DIM	DIMENSIONS			
	INCHES		MM	
	MIN	MAX	MIN	MAX
A	0.006	0.011	0.150	0.300
B	0.043	0.051	1.100	1.300
C	0.059	0.067	1.500	1.700
D	0.016	0.024	0.400	0.600
G	0.035	0.043	0.900	1.100
H	0.059	0.067	1.500	1.700
K	0.021	0.026	0.550	0.650
L	0.004	0.011	0.100	0.300
M	0.004	0.007	0.100	0.180

Note:

- All dimensions are in millimeters (mm) unless otherwise specified.
[所有尺寸均以毫米为单位, 除非另有说明]
- General tolerances: $\pm 0.10\text{mm}$ unless otherwise specified.
[通用公差为 $\pm 0.10\text{mm}$, 除非另有说明]
- Dimensions and tolerances per ASME Y14.5M-2018.
[尺寸和公差遵循 ASME Y14.5M-2018 标准]
- All dimensions shown are exclusive of burrs and gate residues.
Burrs and gate vestiges shall not exceed 0.15 mm in maximum.
[所有尺寸均不包括毛刺和浇口残留。毛刺与浇口残留的尺寸最大不得超过 0.15mm]
- Dimension b does not include dambar protrusion of max 0.100 mm per side.
[尺寸b不包括单边最大0.100 MM的中筋凸出部分]
- Dimensions B and H are the overall extreme outer dimensions of the mold compound. These dimensions exclude mold flash, lead flash, protrusions and burrs but include the maximum allowable mold mismatch.
[B和H是塑封体的外部极限尺寸, 不包括包封溢料、内引线溢料、凸出部分以及胶体毛刺, 但是包含了包封错位的最大尺寸]
- Formed leads shall be planar with respect to one another within a maximum of 0.076 mm relative to the seating plane.
[成型的管脚应为同一平面, 共面性最大为0.1mm]
- ★It is the key size.
[★ 标记为关键尺寸]



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