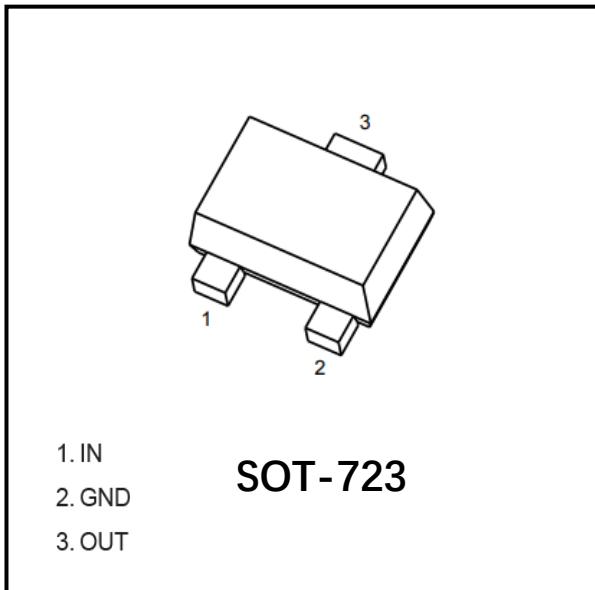


Digital Transistors (Built-in Resistors)



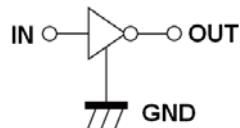
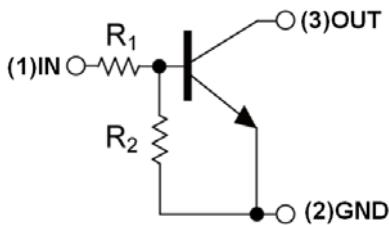
Features

- Epoxy meets UL-94 V-0 flammability rating
- Moisture Sensitivity Level 1
- Built-in bias resistors enable the configuration of an inverter circuit without connecting external input resistors
- Surface mount package ideally Suited for Automatic Insertion
- NPN

Mechanical Data

- **Package:** SOT-723
- **Terminals:** Tin plated leads, solderable per J-STD-002 and JESD22-B102
- **Marking:** E23

■ Equivalent circuit



■ Maximum Ratings (Ta=25°C Unless otherwise specified)

ITEM	SYMBOL	UNIT	CONDITIONS	VALUE
Supply Voltage	V_{CC}	V		50
Input Voltage	V_{IN}	V		-5 to +30
Output Current	I_O	mA		100
Power Dissipation	P_D	mW		100
Junction Temperature	T_J	°C		150
Storage Temperature	T_{STG}	°C		-55 to +150



DTC143ZM

■ Electrical Characteristics (Ta=25°C unless otherwise specified)

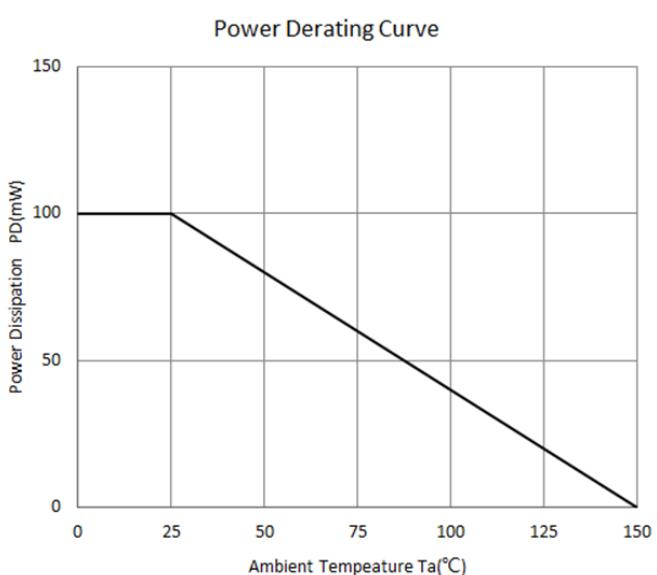
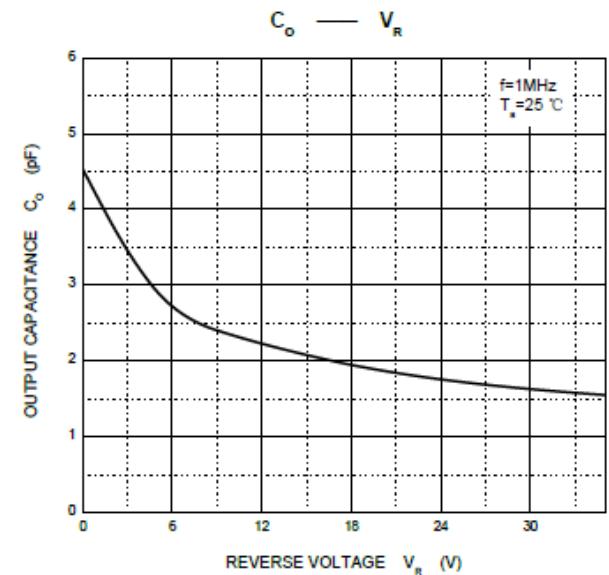
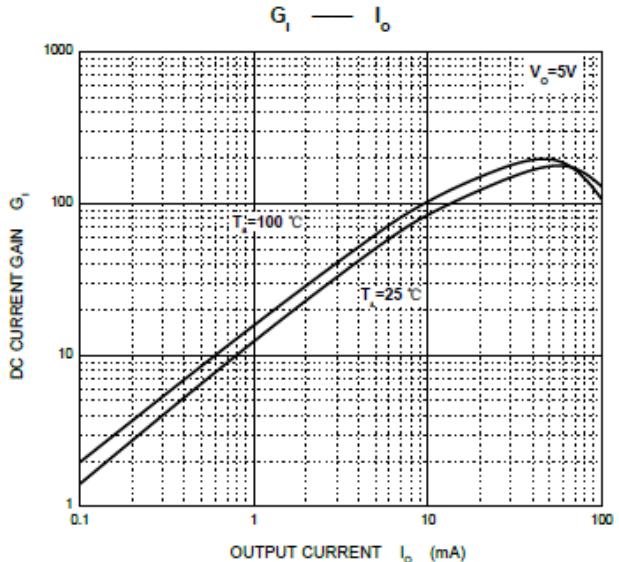
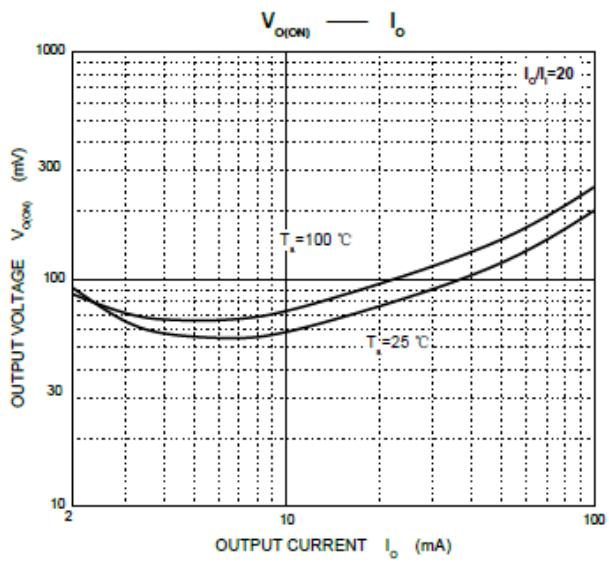
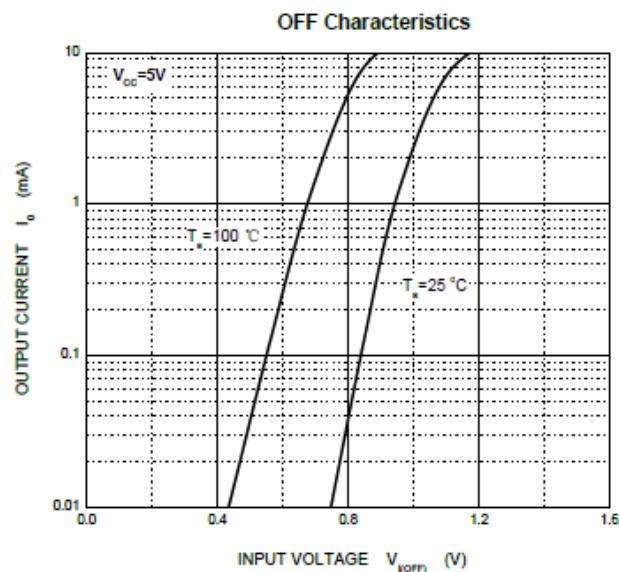
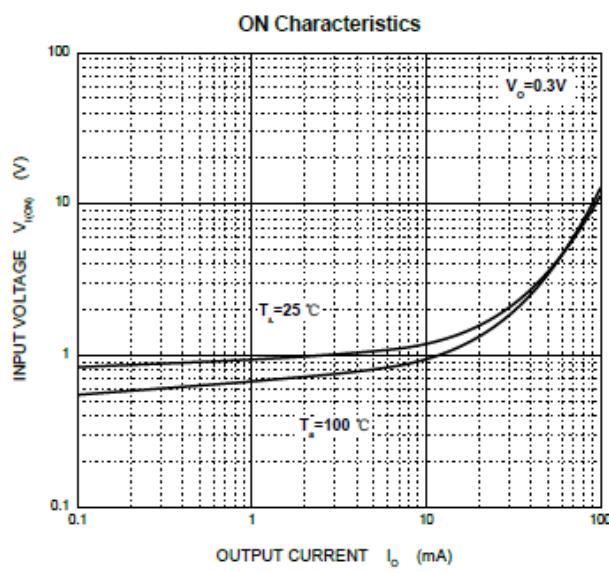
ITEM	SYMBOL	UNIT	CONDITIONS	MIN	TYP	MAX
Input voltage	VI _(off)	V	V _{CC} =5V, I _O =100uA	0.5		
	VI _(on)	V	V _O =0.3V, I _O =5mA			1.3
Output voltage	V _{O(on)}	V	I _O / I _i =10mA/0.5 mA			0.3
Input current	I _i	mA	V _i =5V			1.8
Output current	I _{O(off)}	uA	V _{CC} =50V, V _i =0			0.5
DC current gain	GI		V _O =5V, I _O =10mA	80		
Input resistance	R _i	kΩ		3.29	4.7	6.11
Resistance ratio	R ₂ /R ₁			8	10	12
Transition frequency	f _T	MHz	V _O =10V, I _O =5mA, f=100MHz		250	

■ Ordering Information (Example)

PREFERRED P/N	PACKING CODE	UNIT WEIGHT(g)	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
DTC143ZM	F2	Approximate 0.0013	8000	80000	320000	7" reel

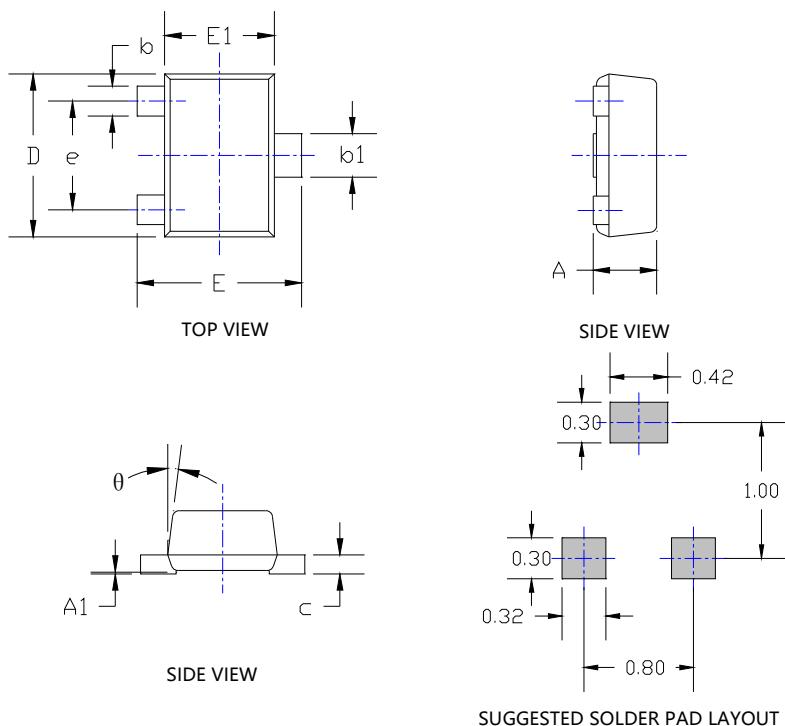


■ Characteristics (Typical)





■SOT-723 Package Outline Dimensions



SYMBOL	INCHES		Millimeter	
	MIN.	MAX.	MIN.	MAX.
A	0.017	0.022	0.430	0.550
A1	0.000	0.002	0.000	0.050
b	0.007	0.011	0.170	0.270
b1	0.011	0.015	0.270	0.370
c	0.003	0.008	0.080	0.200
D	0.045	0.049	1.150	1.250
E	0.045	0.049	1.150	1.250
E1	0.030	0.033	0.750	0.850
e	0.031TYP.		0.800TYP.	
θ	7°REF.		7°REF.	

NOTE:

1. PACKAGE BODY SIZES EXCLUDE MOLD FLASH AND GATE BURRS.
2. TOLERANCE 0.1mm UNLESS OTHERWISE SPECIFIED.
3. THE PAD LAYOUT IS FOR REFERENCE PURPOSES ONLY.

Note:

1. All dimensions are in millimeters (mm) unless otherwise specified.
[所有尺寸均以毫米为单位, 除非另有说明]
2. General tolerances: ±0.10mm unless otherwise specified.
[通用公差为±0.10mm, 除非另有说明]
3. Dimensions and tolerances per ASME Y14.5M-2018.
[尺寸和公差遵循 ASME Y14.5M-2018 标准]
4. All dimensions shown are exclusive of burrs and gate residues. Burrs and gate vestiges shall not exceed 0.15 mm in maximum.
[所有尺寸均不包括毛刺和浇口残留。毛刺与浇口残留的尺寸最大不得超过 0.15mm]
5. Dimension b does not include dambar protrusion of max 0.100 mm per side.
[尺寸b不包括单边最大0.100 MM的中筋凸出部分]
6. Dimensions D and E1 are the overall extreme outer dimensions of the mold compound. These dimensions exclude mold flash, lead flash, protrusions and burrs but include the maximum allowable mold mismatch.
[D和E是塑封体的外部极限尺寸, 不包括包封溢料、内引线溢料、凸出部分以及胶体毛刺, 但是包含了包封错位的最大尺寸]
7. Formed leads shall be planar with respect to one another within a maximum of 0.076 mm relative to the seating plane.
[成型的管脚应为同一平面, 共面性最大为0.1mm]
8. ★It is the key size.
[★ 标记为关键尺寸]



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