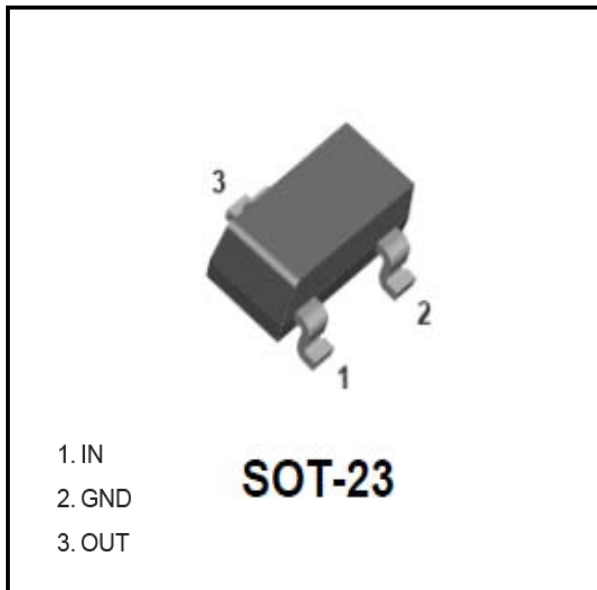


PNP Digital Transistors (Built-in Resistors)



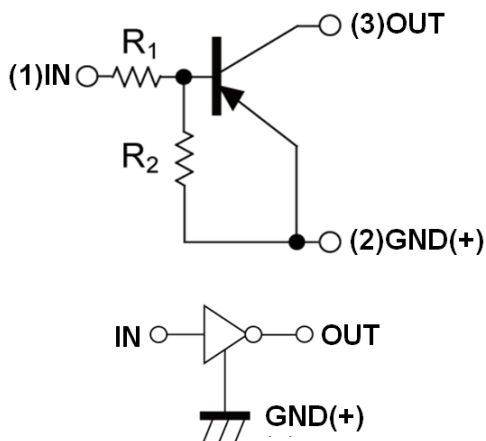
Features

- Epoxy meets UL-94 V-0 flammability rating
- Built-in bias resistors enable the configuration of an inverter circuit without connecting external input resistors
- Surface mount package ideally Suited for Automatic Insertion

Mechanical Data

- **Package:** SOT-23
- **Terminals:** Tin plated leads, solderable per J-STD-002 and JESD22-B102
- **Marking:** P13

■Equivalent circuit



■Maximum Ratings (Ta=25°C Unless otherwise specified)

ITEM	SYMBOL	UNIT	CONDITIONS	VALUE
Supply Voltage	V_{CC}	V		-50
Input Voltage	V_{IN}	V		-40 to +10
Output Current	I_O	mA		-500
Power Dissipation	P_D	mW		200
Junction Temperature	T_J	°C		150
Storage Temperature	T_{STG}	°C		-55 to +150



DDTA114ECA

■ Electrical Characteristics (Ta=25°C unless otherwise specified)

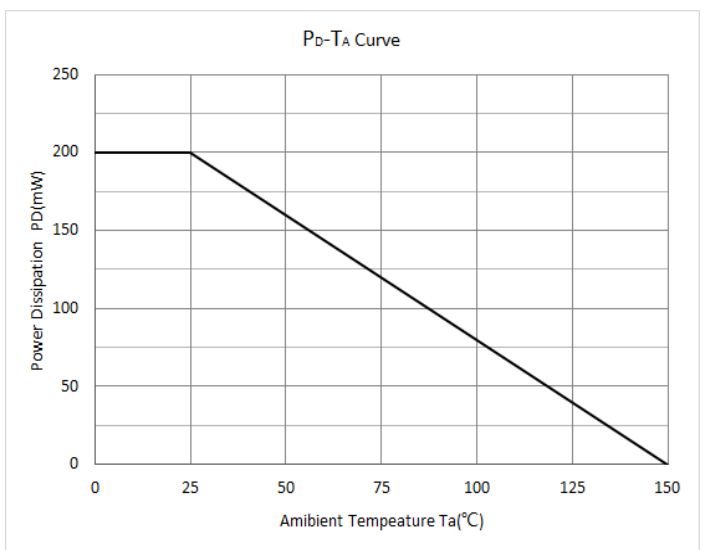
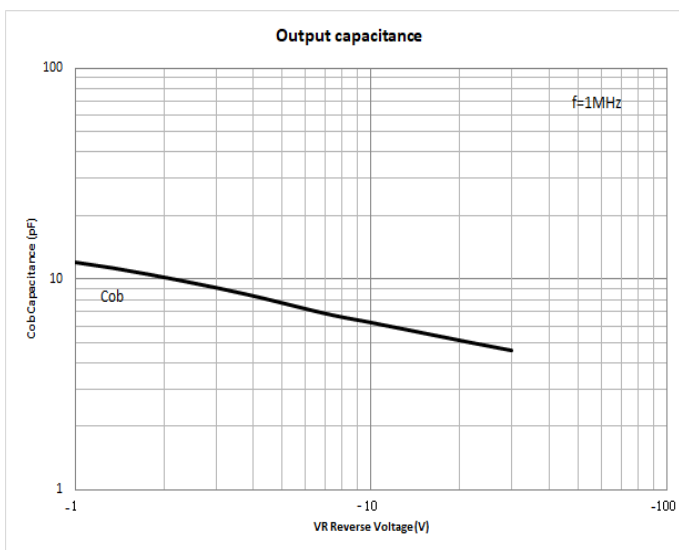
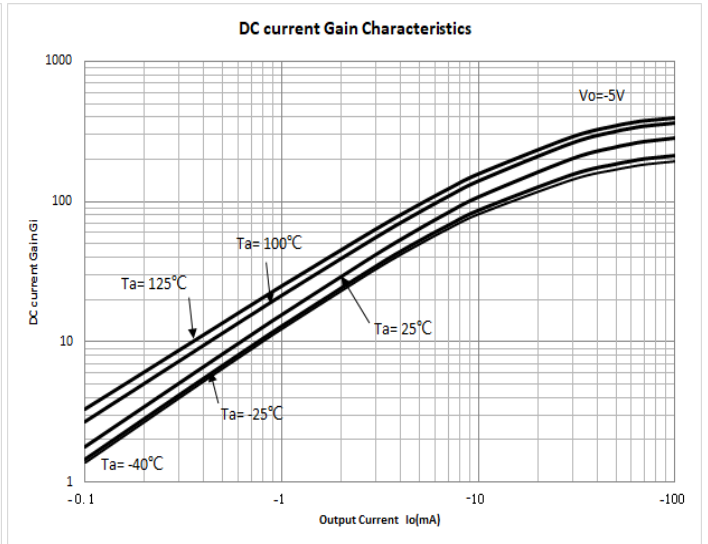
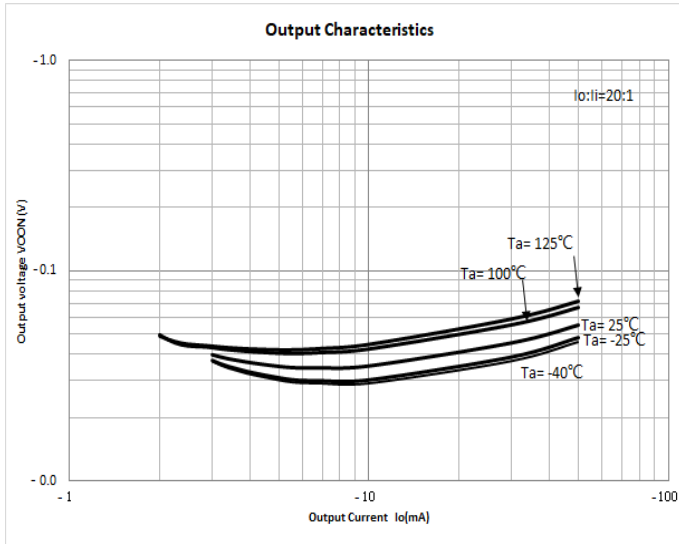
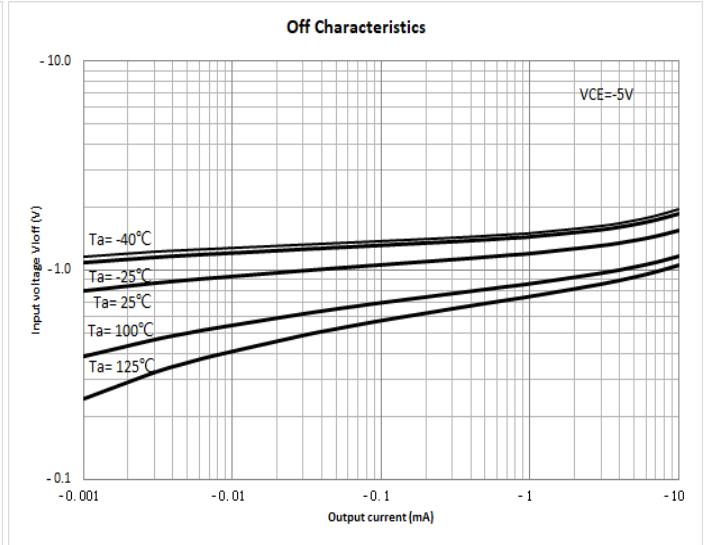
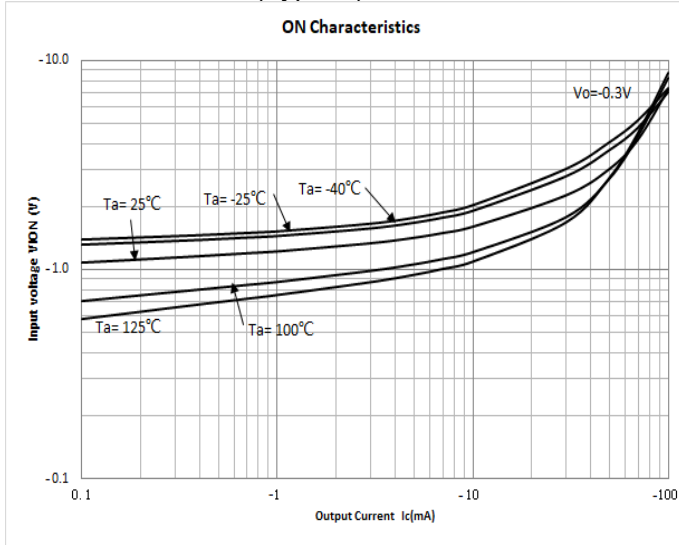
ITEM	SYMBOL	UNIT	CONDITIONS	MIN	TYP	MAX
Input voltage	$V_{I(off)}$	V	$V_{CC}=-5V, I_c=-100\mu A$	-0.5		
	$V_{I(on)}$	V	$V_o=-0.3V, I_c=-10mA$			-3.0
Output voltage	$V_{O(on)}$	V	$I_o / I_i = -50mA / -2.5 mA$			-0.3
Input current	I_I	mA	$V_i = -5V$			-0.88
Output current	$I_{O(off)}$	μA	$V_{CC}=-50V, V_i=0$			-0.5
DC current gain	G_I		$V_o=-5V, I_o = -50mA$	60		
Input resistance	R_i	k Ω		7	10	13
Resistance ratio	R_2/R_1			0.8	1.0	1.2
Transition frequency	fT	MHz	$V_{CE}=-10V, I_E=50mA, f=100MHz$		200	

■ Ordering Information (Example)

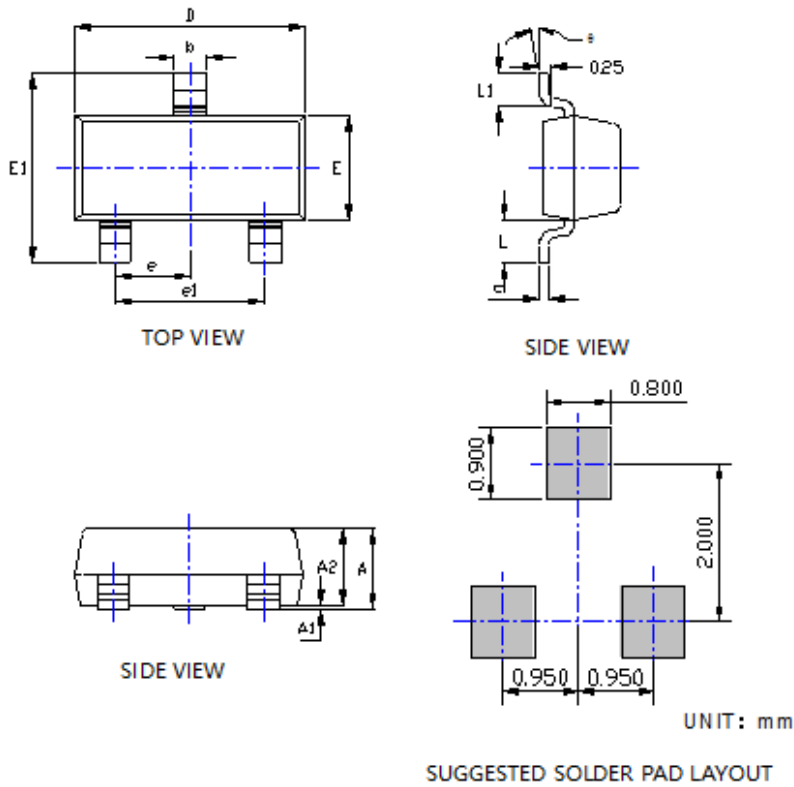
PREFERRED P/N	PACKING CODE	UNIT WEIGHT(g)	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
DDTA114ECA	F2	Approximate 0.009	3000	30000	120000	7" reel



■ Characteristics (Typical)



■SOT-23 Package Outline Dimensions



SYMBOL	DIMENSIONS			
	INCHES		Millimeter	
	MIN.	MAX.	MIN.	MAX.
A	0.035	0.045	0.900	1.150
A1	0.000	0.004	0.000	0.100
A2	0.035	0.041	0.900	1.050
b	0.012	0.020	0.300	0.500
c	0.004	0.008	0.100	0.200
D	0.110	0.118	2.800	3.000
E	0.047	0.055	1.200	1.400
E1	0.089	0.100	2.250	2.550
e	0.037TYP		0.950TYP	
e1	0.071	0.079	1.800	2.000
L	0.022REF		0.550REF	
L1	0.012	0.020	0.300	0.500
θ	0°	8°	0°	8°

NOTE:

1. PACKAGE BODY SIZES EXCLUDE MOLD FLASH AND GATE BURRS.

2. TOLERANCE 0.1mm UNLESS OTHERWISE SPECIFIED.

3. THE PAD LAYOUT IS FOR REFERENCE PURPOSES ONLY.

Note:

1. All dimensions are in millimeters (mm) unless otherwise specified.

[所有尺寸均以毫米为单位，除非另有说明]

2. General tolerances: $\pm 0.10\text{mm}$ unless otherwise specified.

[通用公差为 $\pm 0.10\text{mm}$ ，除非另有说明]

3. Dimensions and tolerances per ASME Y14.5M-2018.

[尺寸和公差遵循 ASME Y14.5M-2018 标准]

4. All dimensions shown are exclusive of burrs and gate residues. Burrs and gate vestiges shall not exceed 0.15 mm in maximum.

[所有尺寸均不包括毛刺和浇口残留。毛刺与浇口残留的尺寸最大不得超过 0.15mm]

5. Dimension b does not include dambar protrusion of max 0.100 mm per side.

[尺寸b不包括单边最大0.100 mm的中筋凸出部分]

6. Dimensions D and E are the overall extreme outer dimensions of the mold compound. These dimensions exclude mold flash, lead flash, protrusions and burrs but include the maximum allowable mold mismatch.

[D和E是塑封体的外部极限尺寸，不包括包封溢料、内引线溢料、凸出部分以及胶体毛刺，但是包含了包封错位的最大尺寸]

7. Formed leads shall be planar with respect to one another within a maximum of 0.076 mm relative to the seating plane.

[成型的管脚应为同一平面，共面性最大为0.1mm]

8. ★It is the key size.

[★ 标记为关键尺寸]



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