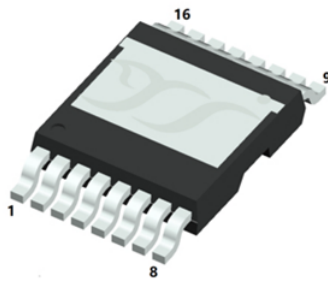
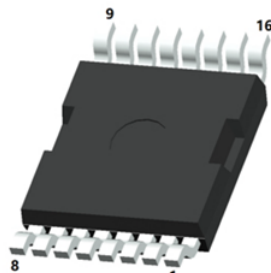


N-Channel Enhancement Mode Field Effect Transistor

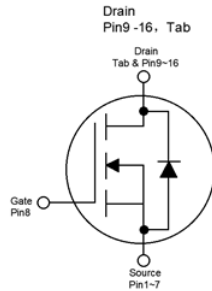


Top View



Bottom View

TOLT



Product Summary

• V_{DS}	100V
• I_D	340A
• $R_{DS(ON)}$ (at $V_{GS}=10V$)	$<1.7m\Omega$
• 100% EAS Tested	
• 100% ∇V_{DS} Tested	
• ESD Level(HBM)	H3A

General Description

- Excellent package for heat dissipation
- High density cell design for low $R_{DS(ON)}$
- Moisture Sensitivity Level 1
- Epoxy Meets UL 94 V-0 Flammability Rating
- Halogen Free
- Part no. with suffix "Q" means AEC-Q101 qualified

Applications

- High power inverter system
- BMS appliances

Limiting Values

Parameter	Conditions		Symbol	Min	Max	Unit
Drain-source Voltage			V _{DS}	-	100	V
Gate-source Voltage			V _{GS}	-20	20	
Continuous Drain Current (Note 1,2)	Steady-State	T _A =25°C,V _{GS} =10V	I _D	-	34	A
		T _A =100°C,V _{GS} =10V		-	24	
Continuous Drain Current (Note 1,3)	Steady-State	T _C =25°C,V _{GS} =10V,Chip limitation		-	340	
		T _C =100°C,V _{GS} =10V		-	240	
Pulsed Drain Current	T _C =25°C,t _p ≤10μs		I _{DM}	-	1360	
Maximum Body-Diode Continuous Current	T _C =25°C		I _S		285	
Avalanche energy (non-repetitive)	T _J =25°C,V _G =10V, R _G =25Ω, L=5mH, I _{AS} =33A		EAS	-	2722.5	mJ
Total Power Dissipation (Note 1,2)	Steady-State	T _A =25°C	P _D	-	4.1	W
		T _A =100°C		-	2	
Total Power Dissipation (Note 1,3)	Steady-State	T _C =25°C		-	416	
		T _C =100°C		-	208	
Junction and Storage Temperature Range			T _J ,T _{STG}	-55	175	°C

Thermal Resistance

Parameter		Symbol	Typ	Max	Units
Thermal Resistance Junction-to-Ambient (Note 2)	Steady-State	$R_{\theta JA}$	-	36	$^{\circ}C/W$
Thermal Resistance Junction-to-Case	Steady-State	$R_{\theta JC}$	-	0.36	



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■ Electrical Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V, I _D =1mA, T _J =25°C	100	-	-	V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =80V, V _{GS} =0V, T _J =25°C	-	-	1	μA
		V _{DS} =80V, V _{GS} =0V, T _J =125°C	-	-	100	
Gate-Source Leakage Current	I _{GSS}	V _{GS} =±20V, V _{DS} =0V, T _J =25°C	-	-	±100	nA
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} , I _D =250μA, T _J =25°C	2	2.6	4	V
Static Drain-Source On-Resistance	R _{DS(ON)}	V _{GS} =10V, I _D =20A, T _J =25°C	-	1.2	1.7	mΩ
Diode Forward Voltage	V _{SD}	I _S =20A, V _{GS} =0V, T _J =25°C	-	0.75	1.2	V
Gate Resistance	R _G	f=1MHz, T _J =25°C	-	1.45	-	Ω
Dynamic Parameters						
Input Capacitance	C _{iss}	V _{DS} =50V, V _{GS} =0V, f=1MHz, T _J =25°C	-	10700	-	pF
Output Capacitance	C _{oss}		-	2010	-	
Reverse Transfer Capacitance	C _{rss}		-	35	-	
Switching Parameters						
Total Gate Charge	Q _g	V _{GS} =10V, V _{DS} =50V, I _D =30A, T _J =25°C	-	166	-	nC
Gate-Source Charge	Q _{gs}		-	34	-	
Gate-Drain Charge	Q _{gd}		-	49	-	
Reverse Recovery Charge	Q _{rr}	I _F =30A, di/dt=100A/μs, V _{GS} =0V, V _R =50V, T _J =25°C	-	167	-	nC
Reverse Recovery Time	t _{rr}		-	92	-	ns
Turn-on Delay Time	t _{D(on)}	V _{GS} =10V, V _{DS} =50V, I _D =30A, R _{GEN} =4.5Ω, T _J =25°C	-	30	-	ns
Turn-on Rise Time	t _r		-	65	-	
Turn-off Delay Time	t _{D(off)}		-	121	-	
Turn-off Fall Time	t _f		-	107	-	

Note:

1. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
2. The value of $R_{\theta JA}$ is measured with the device mounted on the 40mm*40mm*1.1mm single layer FR-4 PCB board with 1 in² pad of 2oz. Copper, in the still air environment with $T_A=25^{\circ}C$. The maximum allowed junction temperature of 175 $^{\circ}C$. The value in any given application depends on the user's specific board design.
3. Thermal resistance from junction to soldering point (on the exposed drain pad).



■ Typical Electrical and Thermal Characteristics Diagrams

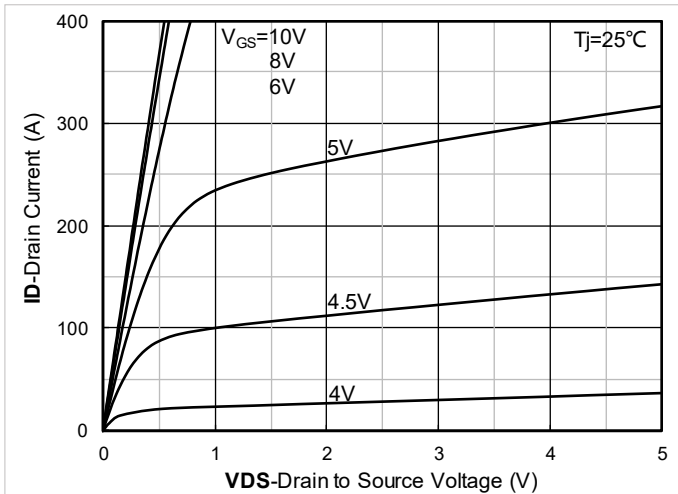


Figure 1. Output Characteristics

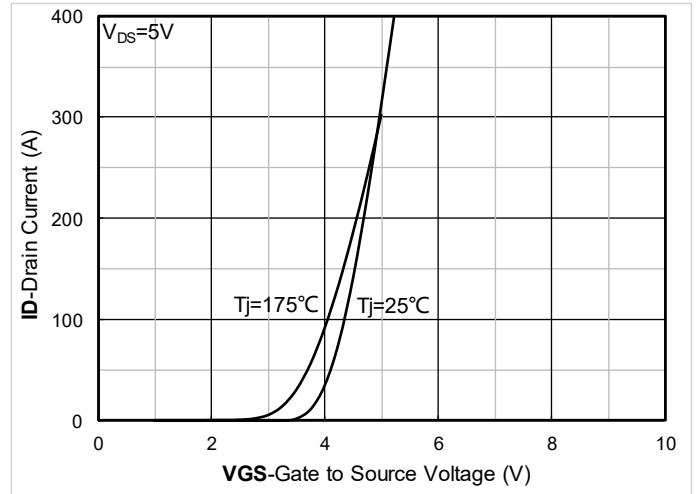


Figure 2. Transfer Characteristics

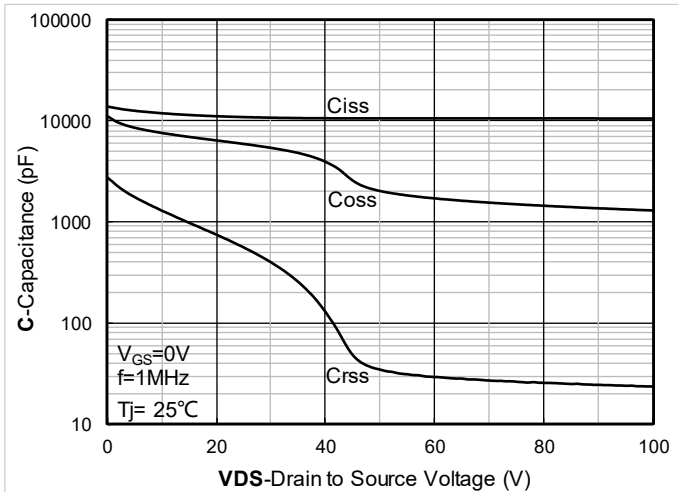


Figure 3. Capacitance Characteristics

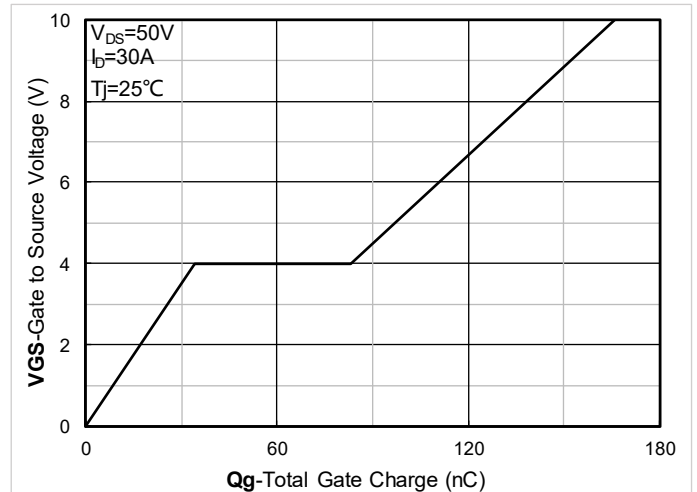


Figure 4. Gate Charge

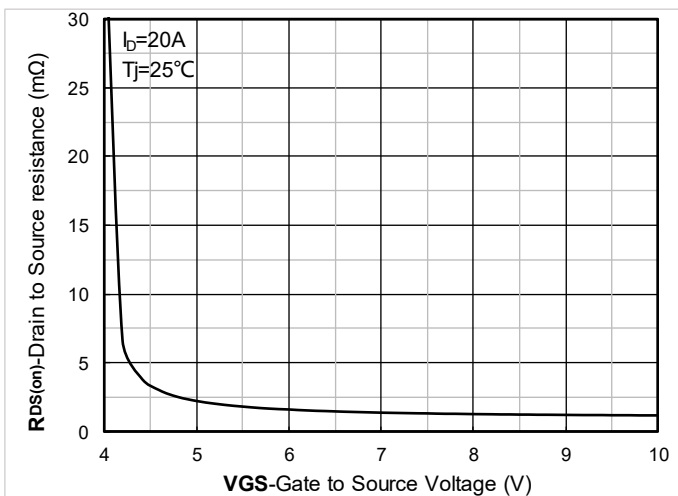


Figure 5. On-Resistance vs. Gate to Source Voltage

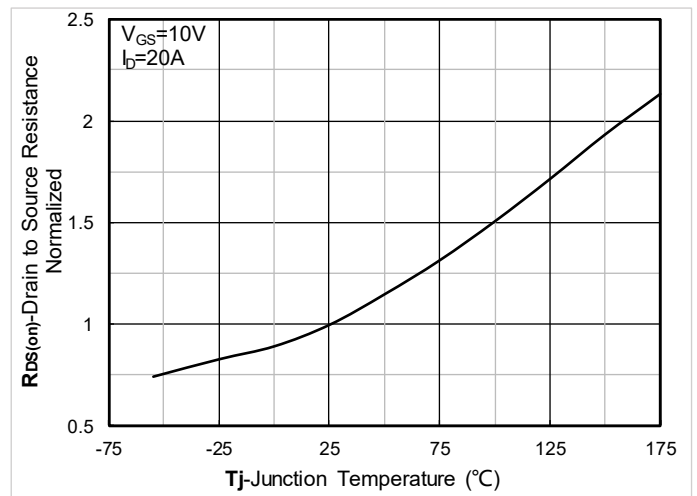


Figure 6. Normalized On-Resistance

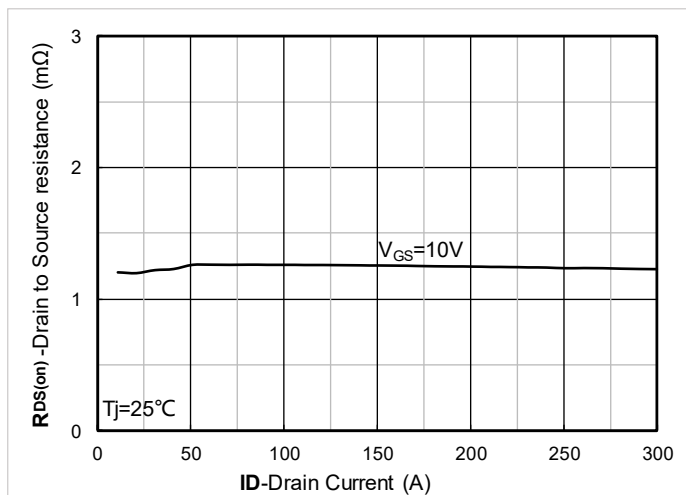


Figure 7. $R_{DS(on)}$ vs. Drain Current

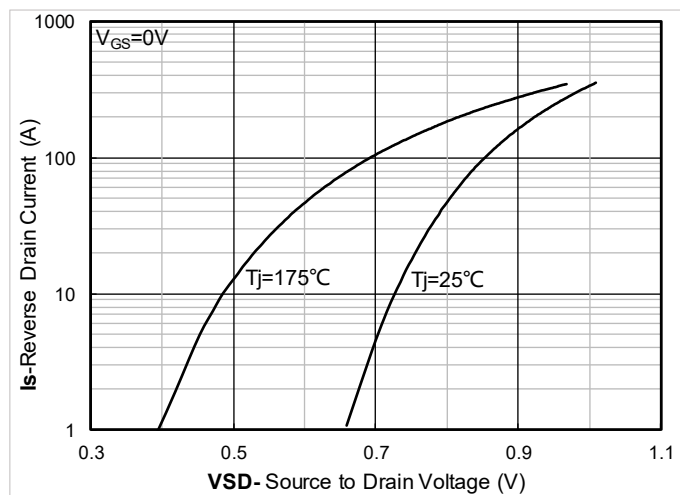


Figure 8. Forward characteristics of reverse diode

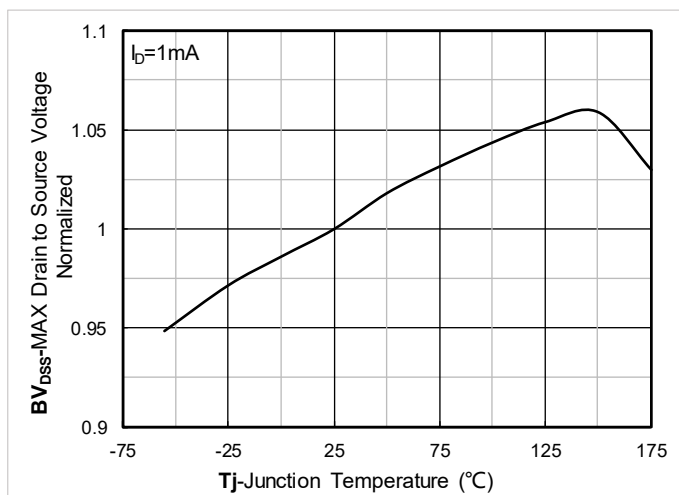


Figure 9. Normalized breakdown voltage

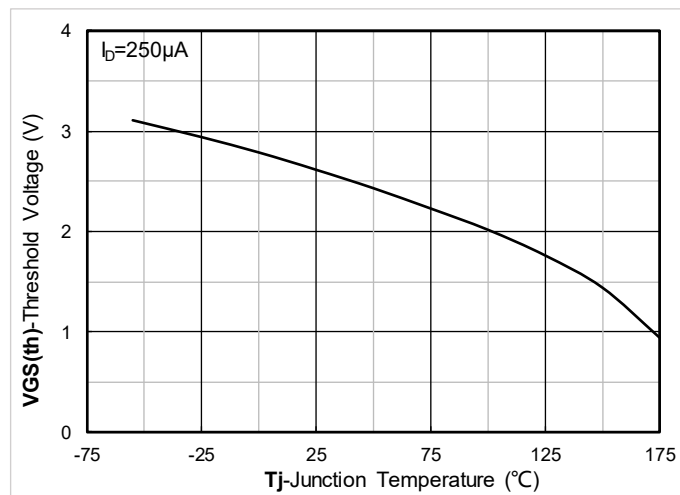


Figure 10. Gate Threshold voltage; typical values

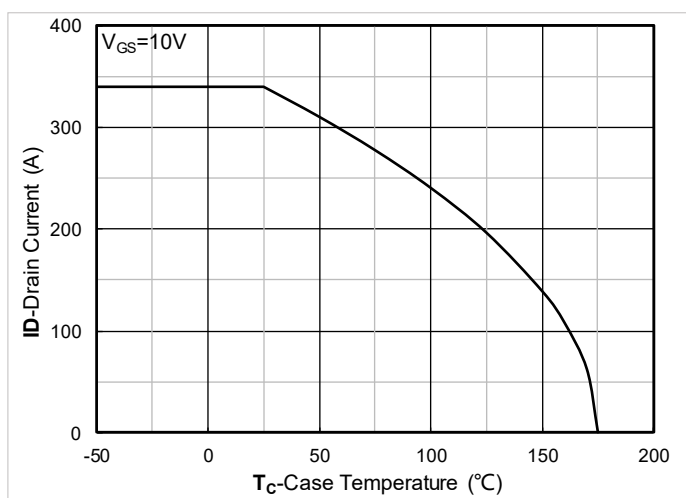


Figure 11. Current dissipation

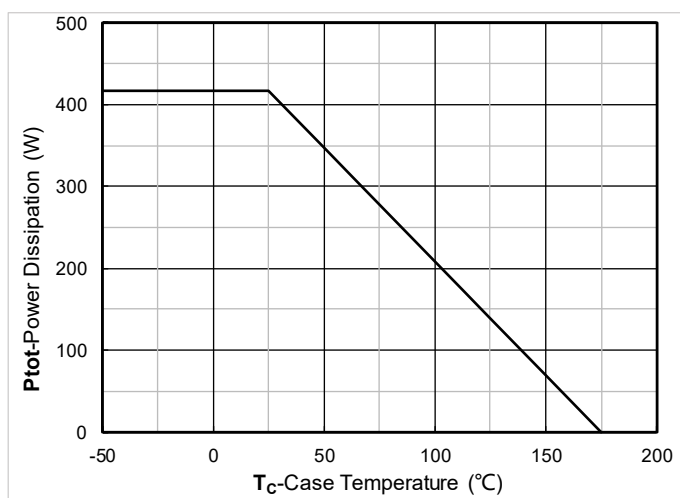


Figure 12. Power dissipation

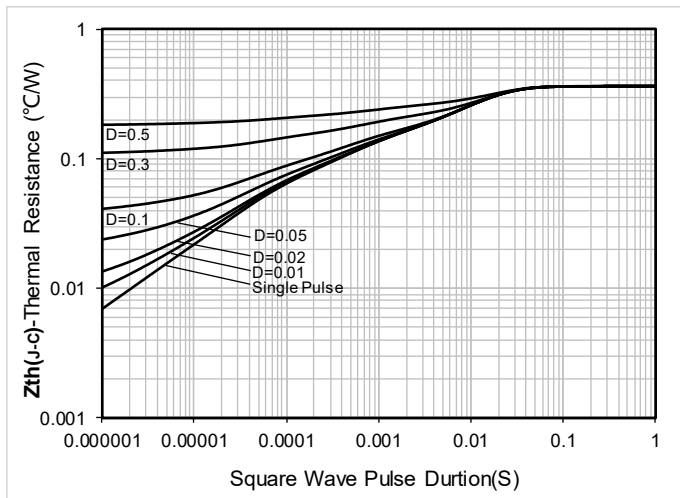


Figure 13. Maximum Transient Thermal Impedance

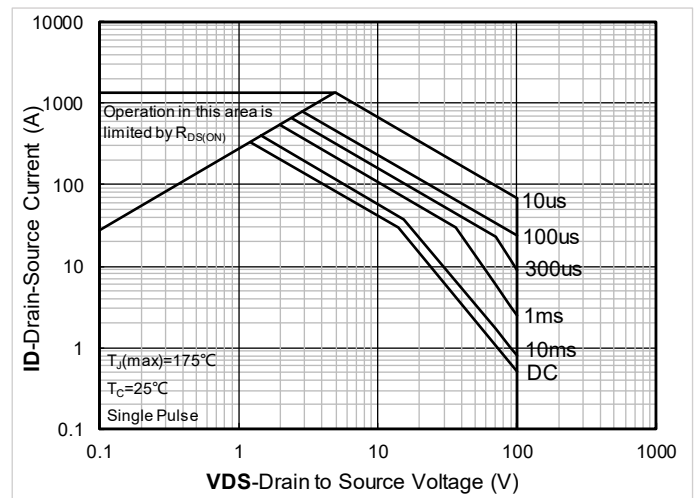


Figure 14. Safe Operation Area

■ Test Circuits & Waveforms

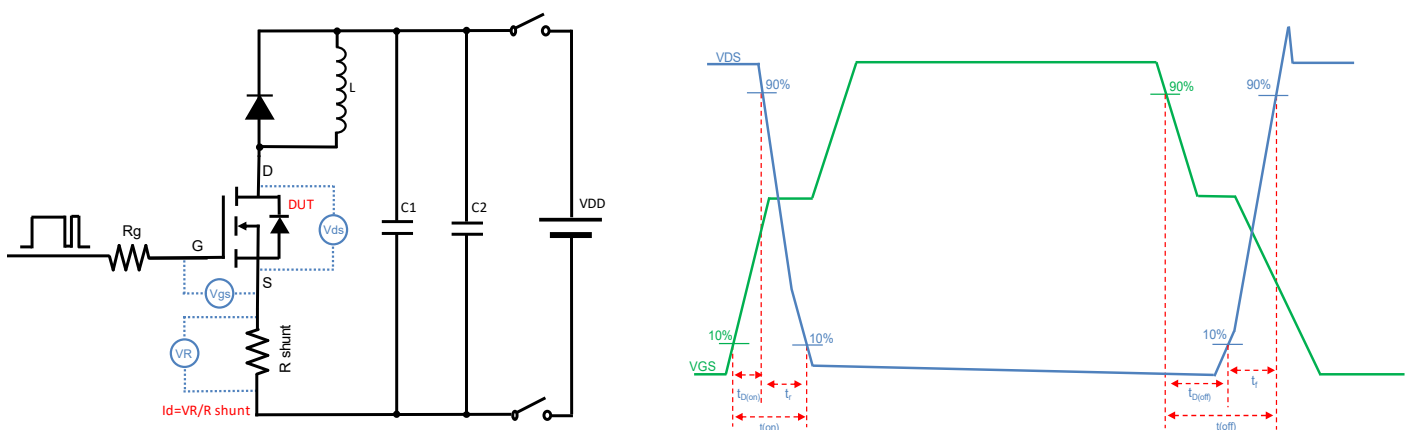
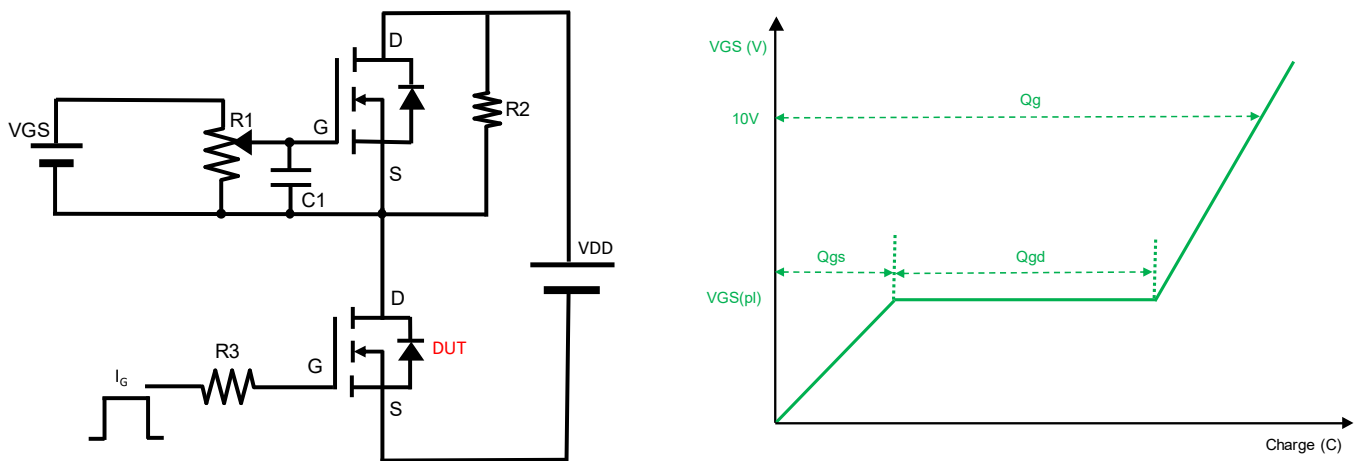
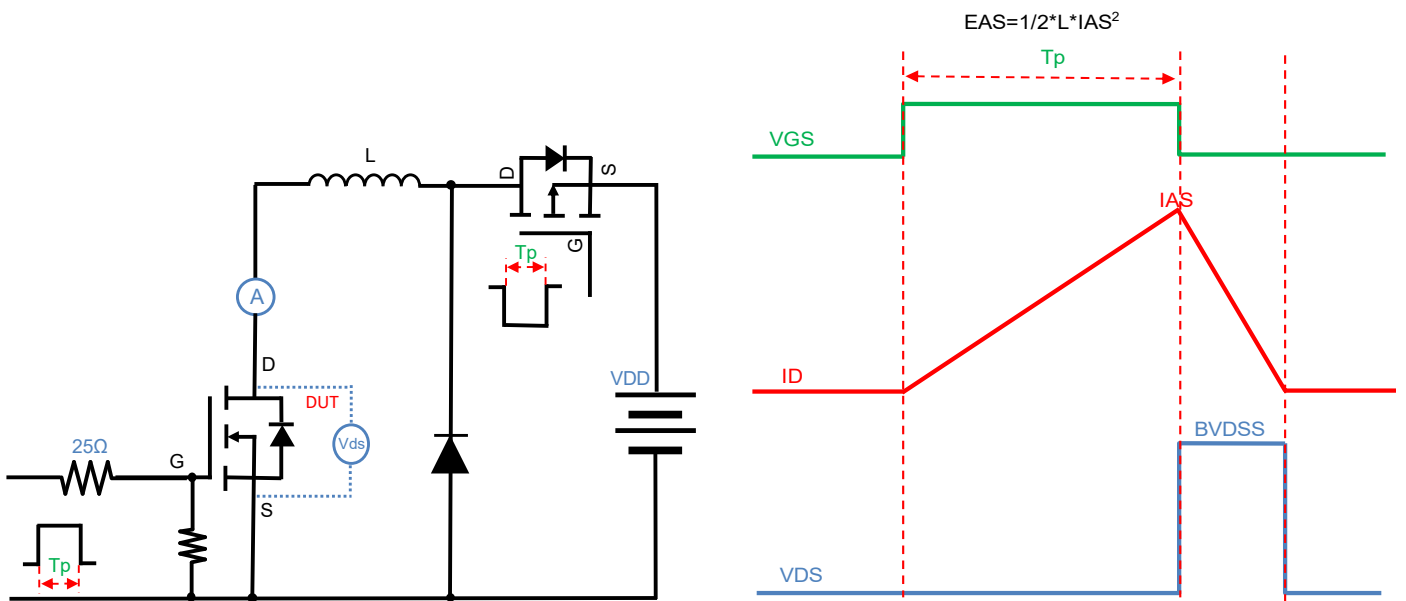


Figure C. Resistive Switching Test Circuit & Waveform

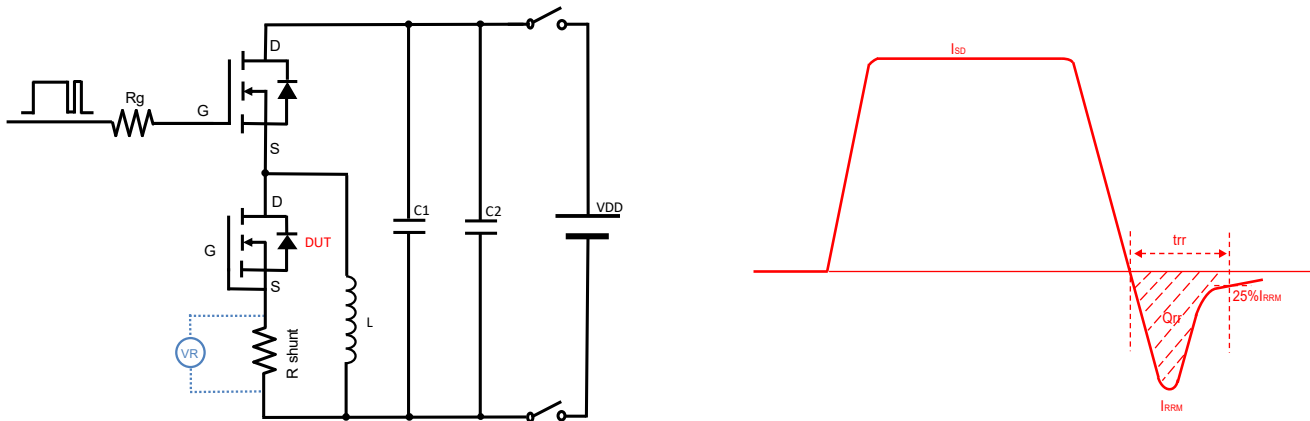
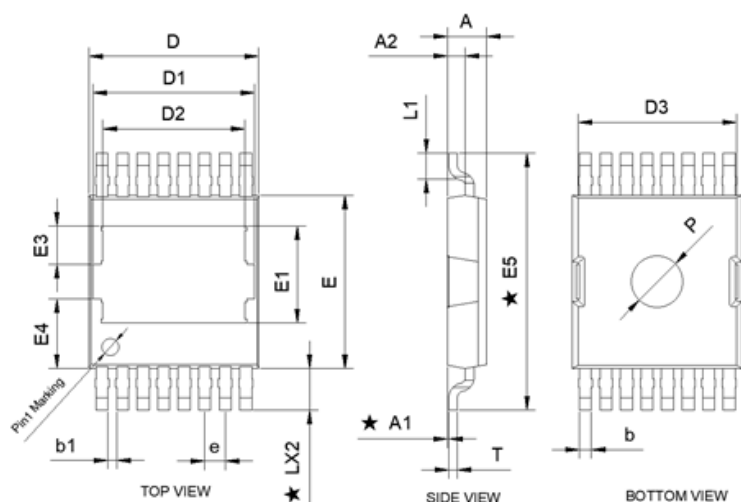


Figure D. Diode Recovery Test Circuit & Waveform



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■ TOLT Package information



SYMBOL	MILLIMETER		
	MIN	NOR	MAX
A	2.25	2.30	2.35
A1	0.01	0.08	0.16
A2	0.99	1.04	1.09
b	0.60	0.70	0.80
b1	0.40	0.50	0.60
D	9.70	9.90	10.10
D1	9.36	9.46	9.56
D2	8.20	8.30	8.40
D3	9.17	9.27	9.37
e	1.20BSC		
E	10.00	10.10	10.30
E1	5.47	5.67	5.87
E2	1.90	2.00	2.10
E3	2.05	2.25	2.45
E4	3.90	4.05	4.20
E5	14.80	15.00	15.20
L	2.20	2.45	2.70
L1	1.51REF		
T	0.458	0.508	0.558
P	2.80	3.00	3.20

Note:

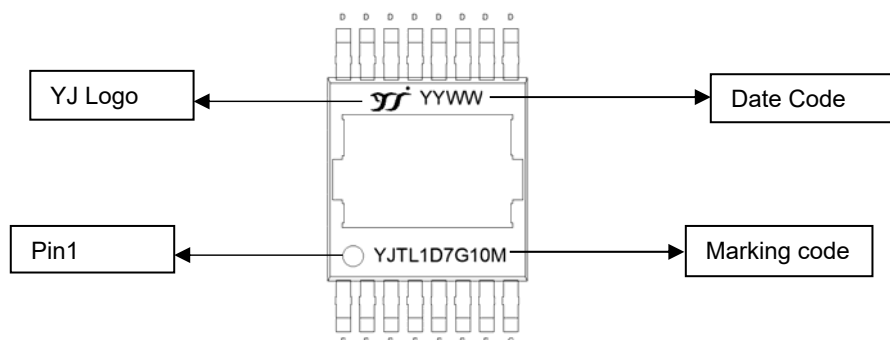
1. Controlling dimension: in millimeters.
2. General tolerance: $\pm 0.10\text{mm}$.
3. The pad layout is for reference purposes only.
4. ★ It is the key size.

SUGGESTED SOLDER PAD LAYOUT



YJTL1D7G10MQ

■ Marking Information



Note:

1. All marking is at middle of the product body
2. All marking is in laser printing
3. YJTL1D7G10M is marking code, YYWW is date code, "YY" is year, "WW" is week
4. Body color: Black



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